MMS Reliability Evaluation Report
RERMCD1412

Qualification of AMKOR second source back-end sites
STM32 in WLCSP- 8" wafers
(PCN 8460- PCN10270)

General Information	
Product division	*MMS MCD*
Package Description	*8" WLCSP*

Locations	
Assembly plant location	*AMKOR Taïwan* *- ATT5 (Bumping)* *- ATT3 (DPS)*
Reliability Evaluation assessment	*PASS*

Reliability tests are performed to assess package integrity under extreme physical and electrical conditions.

They guarantee product/package reliability during end-application manufacturing and operation.

Methodology for product maturity approval has been performed in accordance to STMicroelectronics standard operating procedures (SOP).

Date	Revision	Changes
August 12th, 2014	1.0	Initial release
November 02nd, 2017	1.1	Data for STM32L073xx added for PCN 10270

Approval List			
Function	Site	Name	Date
MMS BE Q&R Responsible	ST Rousset	Antoine GARCIA	Aug 12, 2014
MCD Quality Manager	ST Rousset	Pascal NARCHE	Aug 12, 2014
MCD Quality Manager	ST Rousset	Pascal NARCHE	Nov 02, 2017

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1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

In order to sustain strong demand and in order to provide best-in-class service to his customers, ST MCD Division has decided to increase capacity through double-sourcing for 8" wafers WLCSP assembly.

Target of this reliability evaluation is to qualify AMKOR Taiwan as 2nd 8" wafers WLCSP assembly source:

- Assembly site: AMKOR ATT5
- Test & Finishing site: AMKOR ATT3

3 test vehicles have been identified to cover this reliability evaluation:

- STM32F072xx (TSMC 0.18µm Front-End technology): WLCSP 49 balls
- STM32L151xx (ST F9GO2S Front-End technology): WLCSP 63 balls
- STM32L073xx (ST F9GO2S Front-End technology): WLCSP 49 balls

1.2 Conclusion

All package oriented reliability trials conducted on the 3 test vehicles have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

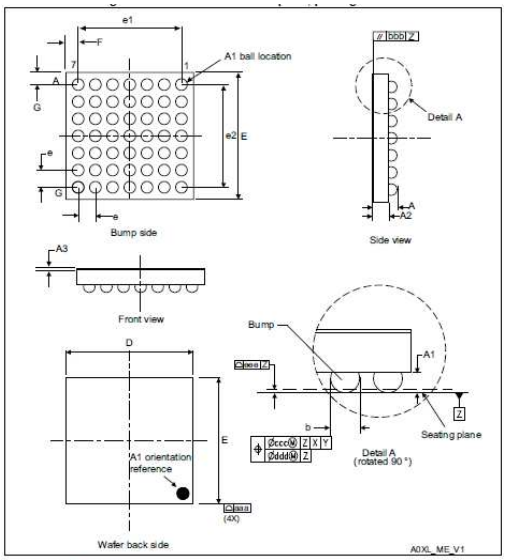
AMKOR Taiwan is qualified as 2nd 8" wafers WLCSP assembly source.

Refer to section 3.1 Reliability Evaluation results summary for reliability evaluation detailed results.

2 PACKAGE CHARACTERISTICS

2.1 Test Vehicle Package description (Abstract from device datasheet):

- **STM32F072xx (TSMC 0.18µm Front-End technology): WLCSP 49 balls 0.4mm pitch**

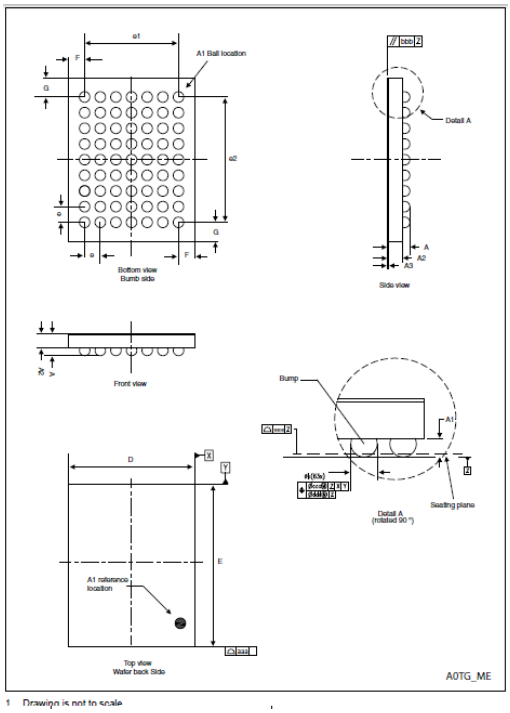


1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3	-	0.025	-	-	0.0010	-
b	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.242	3.277	3.312	0.1276	0.1290	0.1304
E	3.074	3.109	3.144	0.1210	0.1224	0.1238
e	-	0.400	-	-	0.0157	-
e1	-	2.400	-	-	0.0945	-
e2	-	2.400	-	-	0.0945	-
F	-	0.438	-	-	0.0173	-
G	-	0.354	-	-	0.0140	-
N	49					
aaa	-	0.100	-	-	0.0039	-
bbb	-	0.100	-	-	0.0039	-
ccc	-	0.100	-	-	0.0039	-
ddd	-	0.050	-	-	0.0020	-
eee	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

- **STM32L151xx (ST F9GO2S Front-End technology): WLCSP 63 balls 0.4mm pitch**

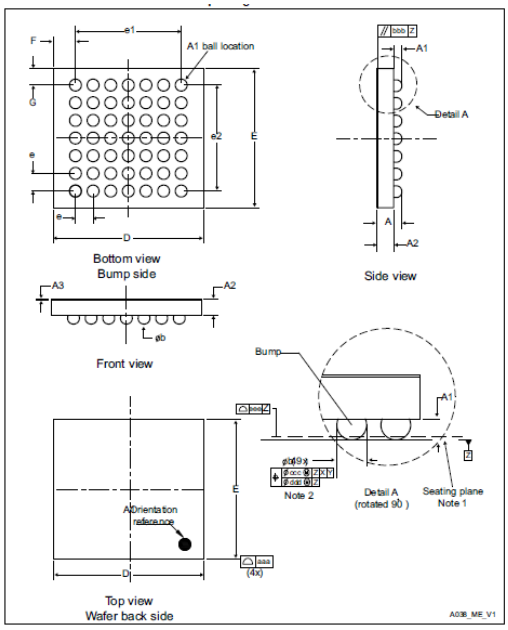


1. Drawing is not to scale

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.540	0.570	0.600	0.0213	0.0224	0.0236
A1		0.190			0.0075	
A2		0.380			0.0150	
A3		0.025			0.0010	
Øb	0.240	0.270	0.300	0.0094	0.0106	0.0118
D	3.193	3.228	3.263	0.1257	0.1271	0.1285
E	4.129	4.164	4.199	0.1626	0.1639	0.1653
e		0.400			0.0157	
e1		2.400			0.0945	
e2		3.200			0.1260	
F		0.414			0.0163	
G		0.482			0.0190	
aaa			0.100			0.0039
bbb			0.100			0.0039
ccc			0.100			0.0039
ddd			0.050			0.0020
eee			0.050			0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

- **STM32L073xx (ST F9GO2S Front-End technology): WLCSP 49 balls 0.4mm pitch**



1. Drawing is not to scale.

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.259	3.294	3.329	0.1283	0.1297	0.1311
E	3.223	3.258	3.293	0.1269	0.1283	0.1296
e	-	0.400	-	-	0.0157	-
e1	-	2.400	-	-	0.0945	-
e2	-	2.400	-	-	0.0945	-
F	-	0.447	-	-	0.0176	-
G	-	0.429	-	-	0.0169	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

2.2 Traceability

2.2.1 Wafer fab information

- **STM32F072xx: WLCSP 49 balls 0.4mm pitch**
  - Wafer fab manufacturing location : TSMC Fab11
  - Silicon process technology: 0.18µm Gen.Emb.Flash logic

- **STM32L151xx: WLCSP 63 balls 0.4mm pitch**
  - Wafer fab manufacturing location : ST Rousset
  - Silicon process technology : F9GO2S (CMOSF9S)

- **STM32L073xx: WLCSP 49 balls 0.4mm pitch**
  - Wafer fab manufacturing location : ST Rousset
  - Silicon process technology : F9GO2S (CMOSF9S)

2.2.2 Assembly information

- **STM32F072xx:**
  - Assembly site : AMKOR Taïwan
    - Bumping : ATT5
    - Test & finishing : ATT3
  - Package description : WLCSP49 0.4mm pitch
  - Die thickness after back-grinding : 355+/-12.5 µm
  - Balls material & diameter : SACN125 (balls raw diameter 230µm)
  - Passivation material : Polyimide
  - Redistribution material : Copper RDL + TiW/Cu/Cu UBM
  - Back side coating material : PET film
  - Package Moisture Sensitivity Level (JEDEC J-STD020D): MSL1

- **STM32L151xx:**
  - Assembly site : AMKOR Taïwan
    - Bumping : ATT5
    - Test & finishing : ATT3
  - Package description : WLCSP63 0.4mm pitch
  - Die thickness after back-grinding : 355+/-12.5 µm
  - Balls material & diameter : SACN125 (balls raw diameter 250µm)
  - Passivation material : Polyimide
  - Redistribution material : Copper RDL + TiW/Cu/Cu UBM
  - Back side coating material : PET film
  - Package Moisture Sensitivity Level (JEDEC J-STD020D): MSL1

- **STM32L073xx:**

  - Assembly site : AMKOR Taïwan
    - Bumping : ATT5
    - Test & finishing : ATT3
  - Package description : WLCSP49 0.4mm pitch
  - Die thickness after back-grinding : 355+/-12.5 µm
  - Balls material & diameter : SACN125 (balls raw diameter 230µm)
  - Passivation material : Polyimide
  - Redistribution material : Copper RDL + TiW/Cu/Cu UBM
  - Back side coating material : PET film
  - Package Moisture Sensitivity Level (JEDEC J-STD020D): MSL1

3 RELIABILITY EVALUATION PLAN/ RESULTS

Package integrity of test vehicles described in above section has been evaluated through below reliability trials.

3.1 Reliability Evaluation results summary

Reliability trials have been performed on 4 assembly lots:

Die	Device	Package	Reduced Rawline	Number of lots	RELIS ref
448	STM32F072x	WLCSP49	3D*448	2	GRAL1414001/1414002
427	STM32L151xx	WLCSP63	TB*427	2	GRAL1414003/1414004
447	STM32L073xx	WLCSP49	51*447	1	GRAL1737003

Package oriented trials - Short description						Results				
Descript.	***Test/Method***	***Conditions***	***Sample Size***	***Criteria***	***Read out /Duration***	***Lot 1***	***Lot 2***	***Lot 3***	***Lot 4***	***Lot 5***
						448	448	427	427	447
ESD Charge Device Model										
ESD CDM	ANSI/ESD STM5.3.1	N.A	3 X 2	Class 3	250V	0/3	-	-	-	
				Class 4	500V	-	-	0/3	-	0/3
Preconditioning: moisture sensitivity level 1										
PC	J-STD-020D JESD22-A113	24h bake @ 125°C 168h @ 85°C / 85% RH Reflow simulation (3 times) @ 260°C peak temperature	308 X 4	A0/R1 (*)		0/308	0/308	0/308	0/308	NA
Temperature Humidity Bias after Preconditioning										
THB	JESD 22-A101	85°c, 85% RH	77 X 4	A0/R1 1000h	1000h	0/77	0/77	0/77	0/77	NA
Unbiased HAST after Preconditioning										
UHAST	JESD 22-A118	Ta=130°c 85%RH	77 X 4	A0/R1 96h	96h	0/77	0/77	0/77	0/77	NA
Thermal Cycling after Preconditioning										
TC	JESD 22-A104	-65°c/+150°c	77 X 4	A0/R1 1000cy	500cy	0/77	0/77	0/77	0/77	NA
High Temperature Storage Life after Preconditioning										
HTSL	JESD 22-A103	150°c	77 X 4	A0/R1 1000h	1000h	0/77	0/77	0/77	0/77	NA

(*) A0/R1: Accepted if 0 reject/ Rejected if 1 reject.

3.2 Package oriented tests

3.2.1 Trials description

3.2.1.1 Preconditioning (PC)

According to ST spec 0098044.
Preconditioning test sequence simulates storage and soldering of SMD (surface mount devices) before submitting them to the reliability tests. It aims to validate the moisture sensitivity level of the package, and prepare it to the stress of additional reliability tests, thus enabling a good modelization of the life of the packaged product.
Out-of-bag floor life storage and soldering are modeled by the following test sequence:

- Bake to completely remove moisture from the package;
- Moisture soak according to the package moisture level;
- IR reflow.

The aim is to check that the chip and plastic package withstand the stress due to report on card. Depending on their technology, packages may absorb moisture during their transportation and/or storage, moisture that is released during the soldering operation. At this step, the moisture absorbed is vaporized due to high temperature of solder report process. This phenomenon can create plastic swelling, "pop corn" effect, and cracks which eventually results in wire breakage, passivation cracks, and delamination.

3.2.1.2 Unbiased Highly Accelerated Stress Test (uHAST)

The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solidstate devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is is used to identify failure mechanisms internal to the package and is destructive.

3.2.1.3 High Temperature Storage Life (HTSL)

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.

Purpose: to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.

3.2.1.4 Temperature Cycling (TC)

The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere (thermal gradient typical 10 C/min).

Purpose: to investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system.

Typical failure modes are linked to metal displacement, dielectric cracking, moulding compound delamination, wire-bonds failure, die-attach layer degradation.

3.2.1.5 Temperature Humidity Bias (THB)

The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.

The Temperature Humidity Bias follows the same method than HAST at lower temperature.

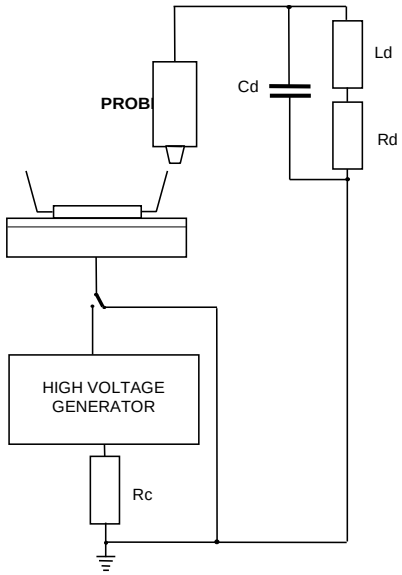
Purpose: to investigate failure mechanisms activated in the die-package environment by electrical field and wet conditions.
Typical failure mechanisms are electro-chemical corrosion and surface effects related to the molding compound.
The package moisture resistance with electrical field applied is verified, both electrolytic and galvanic corrosion are put in evidence.

Conditions:

- Ta=85°C; R.H.=85%;
- Power supply voltage less or equal to max operative voltage to not exceed Tj = 95 °C.

3.2.1.6 ESD Charge Device Model (CDM)

This ESD failure model is associated with the device and package itself. The CDM is intended to simulate charging/discharging events that occur in production equipment and processes. The Field induced CDM equivalent circuit used to describe this phenomenon is illustrated in Figure 1.



Possible (but not exhaustive) values of impedance:

Rc ≥ 100 MΩ
Rd = 1 - 10 Ω
Ld = 5 nH
Cd = 10 pF

Fig.1 : Field induced CDM equivalent circuit

4 APPLICABLE AND REFERENCE DOCUMENTS

- ADCS 0061692: RELIABILITY TESTS AND CRITERIA FOR QUALIFICATIONS
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.7: Product Maturity Level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.6.11: Program management for product qualification
- SOP 2.6.19: Process maturity level

- ANSI-ESD STM5.3.1: Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)

- JESD22-A103: High temperature storage life
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A118: Accelerated moisture resistance - unbiased hast
- JESD22-A104: Temperature cycling

5 GLOSSARY

ESD CDM	Electrostatic discharge (charge device model)
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
UHAST	Unbiased HAST
HTSL	High temperature storage life

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PRODUCT/PROCESS CHANGE NOTIFICATION
PCN 10270 – Additional information

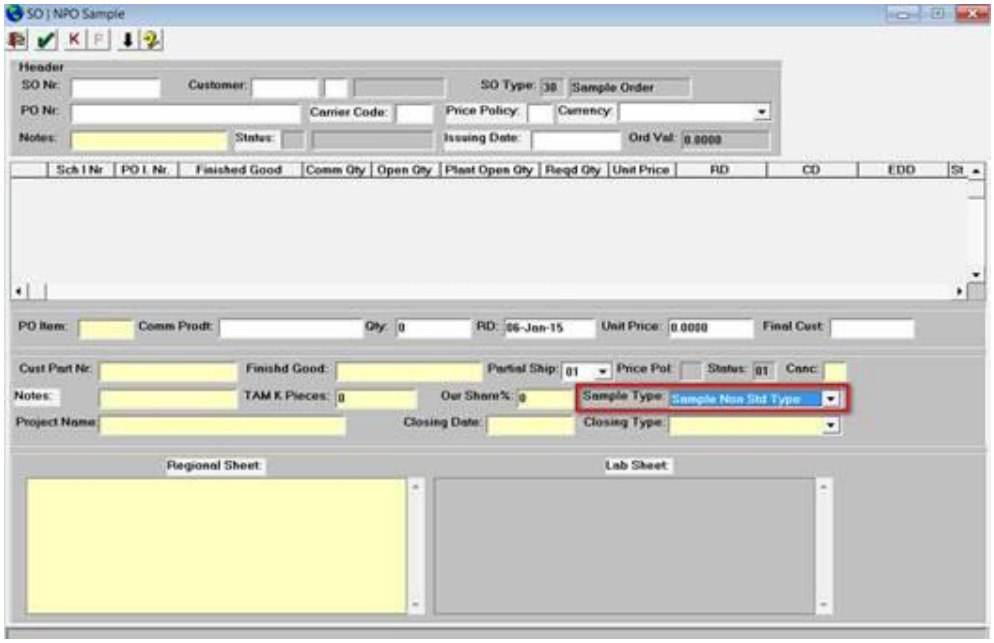
Additional Amkor ATT (Taiwan) back-end site – STM32L073x 192K products in WLCSP package

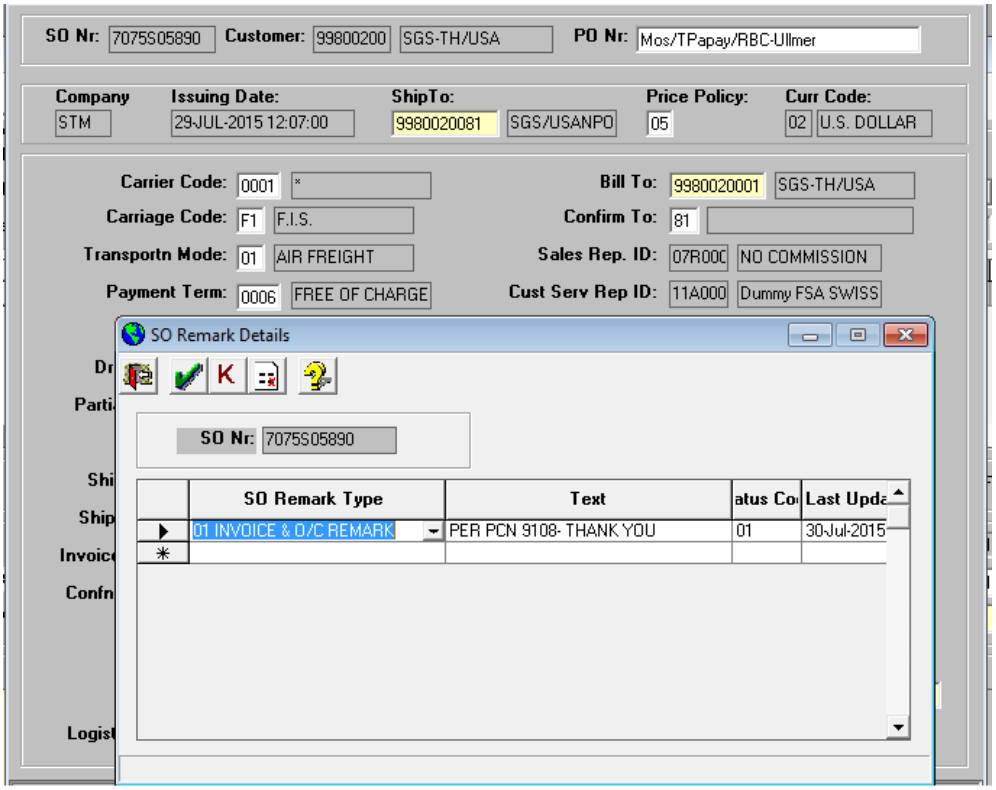
MDG - Microcontrollers Division (MCD)

How to order samples?

For all sample request linked to this PCN, please:

- request sample(s) through Notice tool, indicating a single Commercial Product for each request.
- insert “PCN 10270” into the remarks of your order.
- place **non standard** sample order using the following field in your system.

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